Design Overview Of The

Space Shuttle Orbiter
Modular Memory Unit

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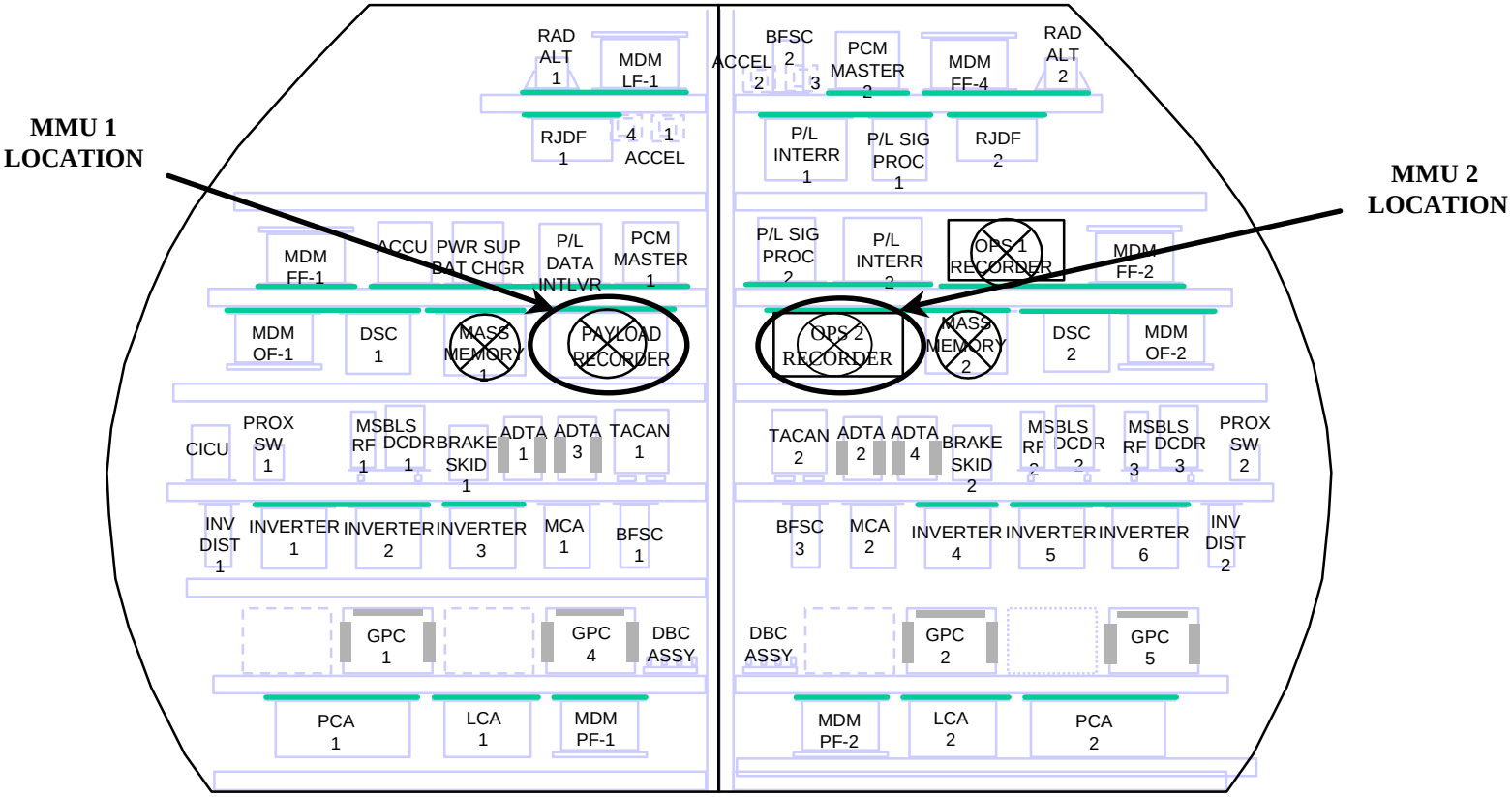
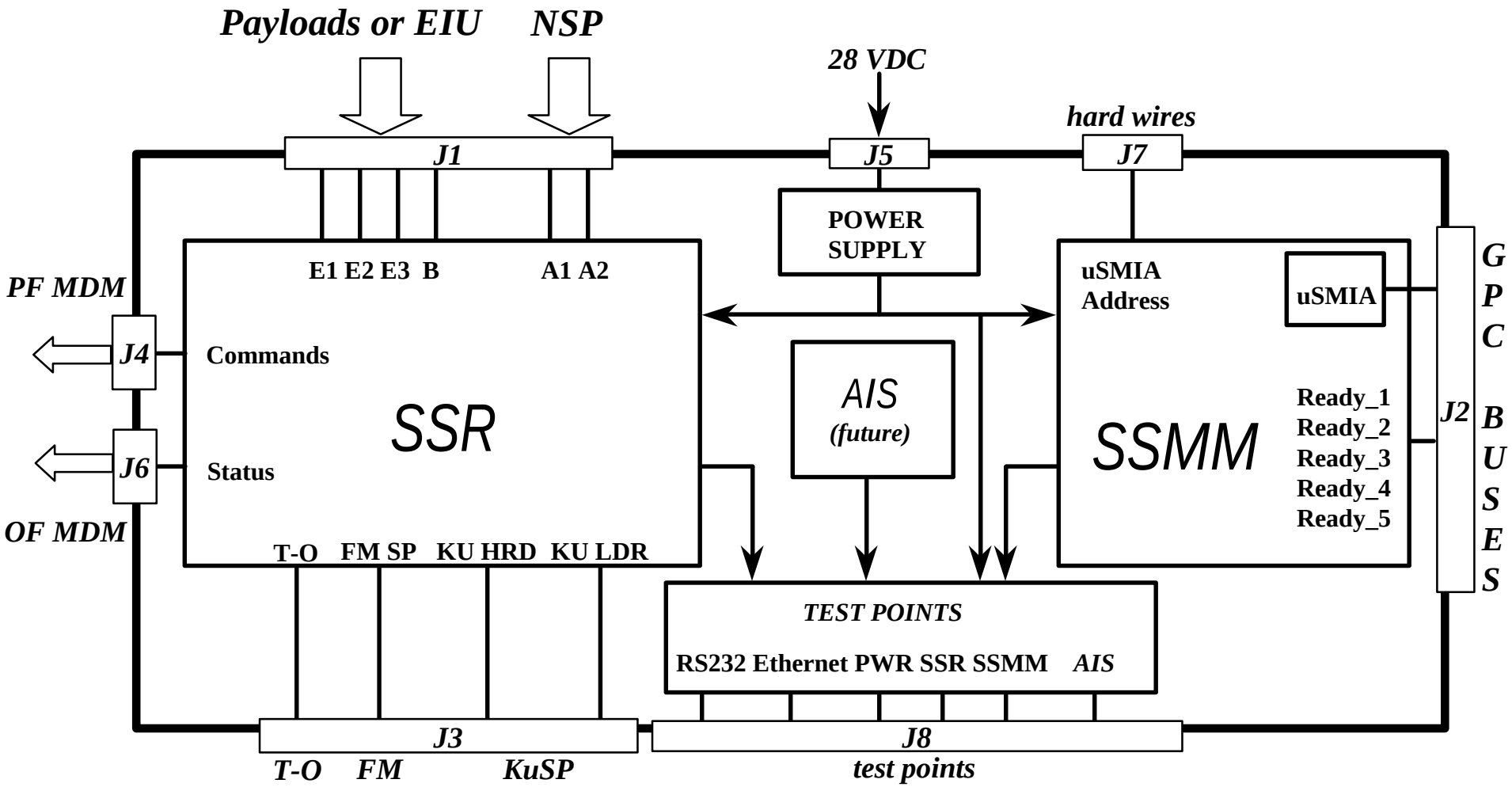
System Level Overview

- **Two Modular Memory Unit (MMU) LRU's Per Orbiter**
  - Located In The Forward Avionics Bay 1 And Bay 2
- **Each MMU Combines Payload Recorder, OPS Recorder, and Mass Memory Unit (MMU) Functions Into A Single LRU**
- **Solid State Recorder (SSR) Function Replaces OPS and Payload Recorders**
  - Operational Instrumentation (OI)Data
    - OPS Recorder Function
  - Space Shuttle Main Engine Data from Engine Interface Unit(s)
    - OPS Recorder Function
  - Digital Payload Data
    - Previous Payload Recorder Function
    - Analog data recording no longer supported
  - Commands And Status Through MDM Interfaces
- **Solid State Mass Memory (SSMM) Function Replaces Current Mass Memory Unit**
  - Current Mass Memory Functions (PASS, BFS, etc.)
  - Transparent With Current Mass Memory Operation With Exception Of:
    - Flash Memory Read/Write Versus Mechanical Tape Operation
    - Bite Bits And Interpretation Of Bite Results

Vehicle Installation



Simplified MMU/Orbiter Interfaces



MMU Interfaces And Data Rates

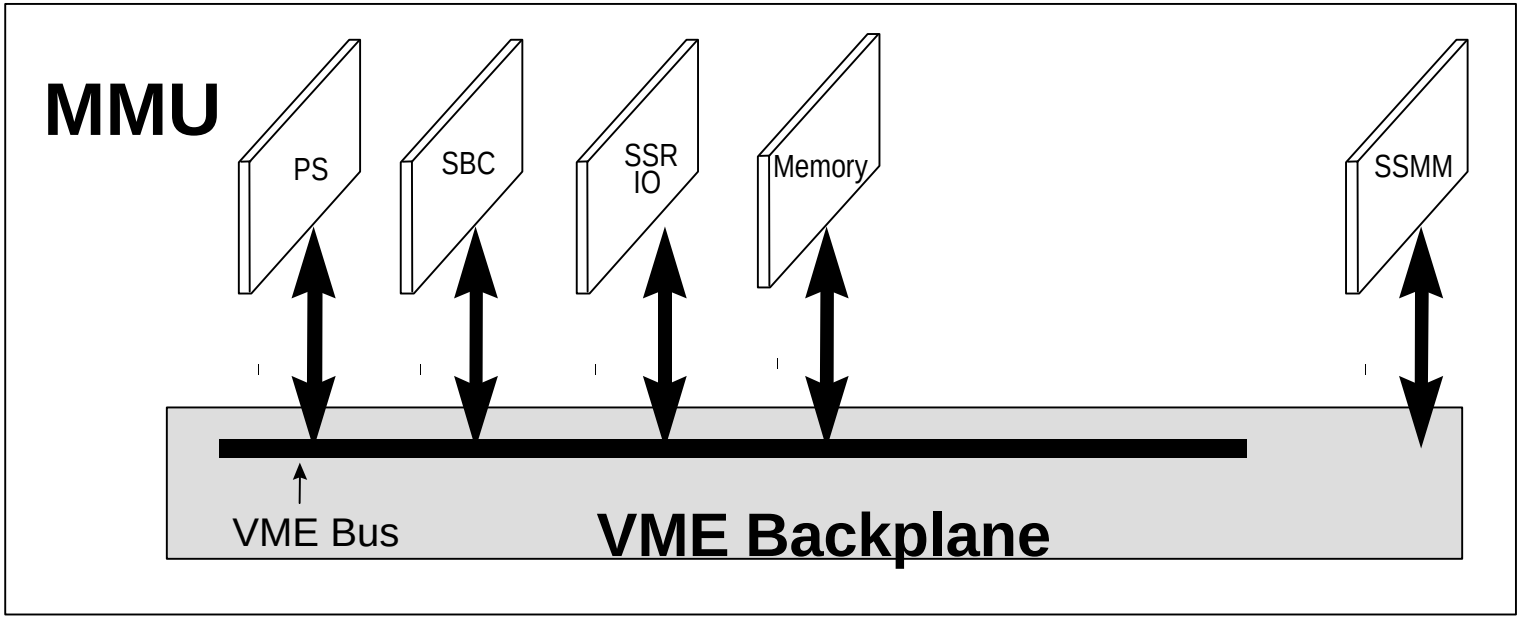
Location	Input	Description	Record Rate (Kbps)	Playback Rate (Kbps)
Av Bay 1	A1/A2	NSP 1 or NSP 2	96, 128 & 192	960, 1024 & 2048
Av Bay 1	B	payload (IUS, Spacelab, etc.)	32 - 1000 kb/s	960, 1024 & 2048
Av Bay 1	E1	payload (OARE, etc.)	32 - 1000 kb/s	960, 1024 & 2048
Av Bay 1	E2	Spare	32 - 1000 kb/s	960, 1024 & 2048
Av Bay 1	E3	Spare	32 - 1000 kb/s	960, 1024 & 2048
Av Bay 2	A1/A2	NSP 1 or NSP 2	96, 128 & 192	960, 1024 & 2048
Av Bay 2	B	Spare	32 - 1000 kb/s	960, 1024 & 2048
Av Bay 2	E1	EIU1	60	960
Av Bay 2	E2	EIU2	60	960
Av Bay 2	E3	EIU3	60	960

- **Each MMU Is Capable Of Supporting:**
  - **Simultaneous Recording Up To Four Parallel Inputs (E1, E2, E3 And A)**
    - **"Auto Detect" Rate At Each Input Channel**
  - **Simultaneous Recording And Playback Operation**
    - **Playback Rate Is "User Specified"**

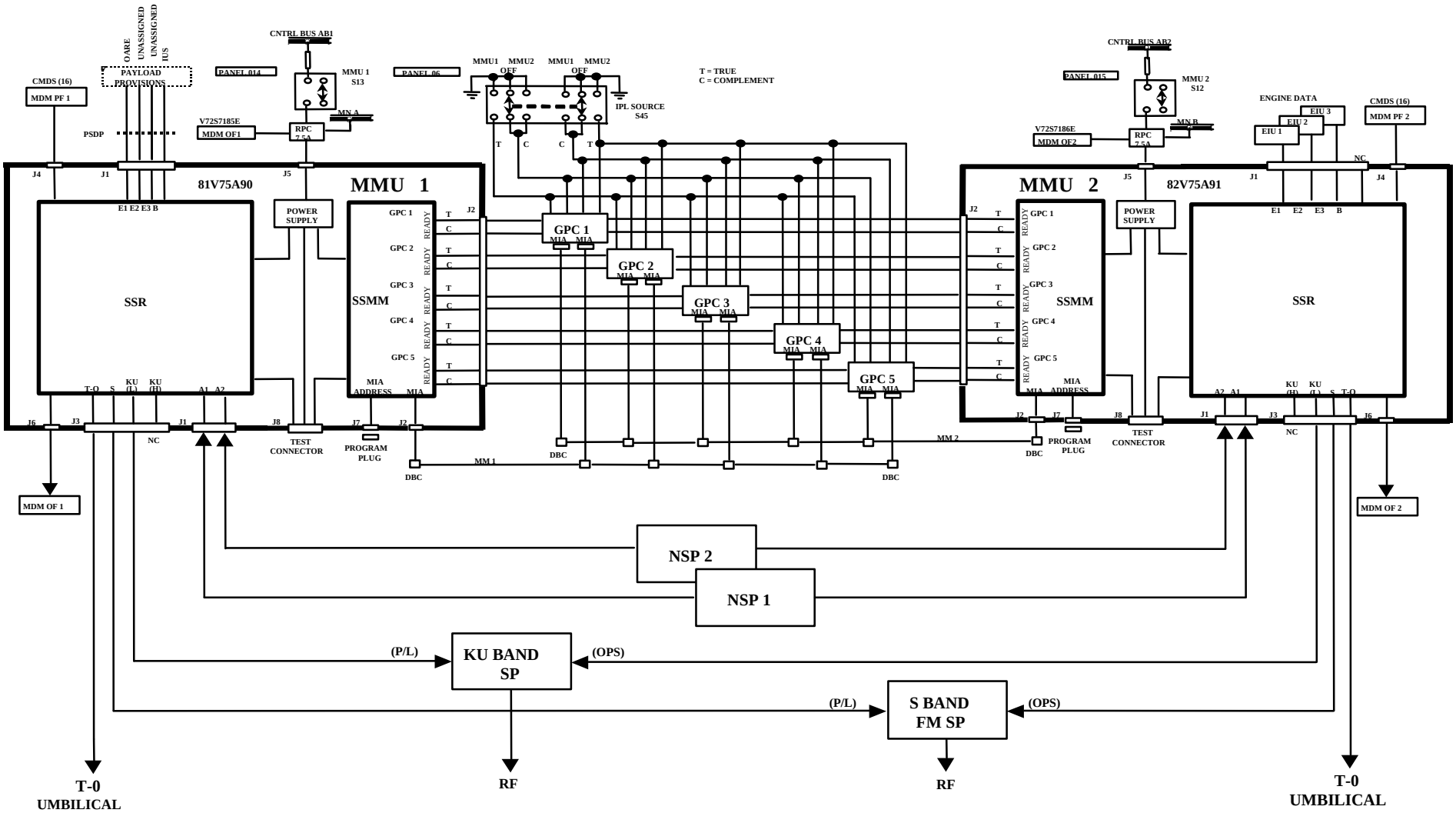
LRU Overview

- **Conduction Cooling VME64x-Based Design With 250 W Power Supply**
- **Includes following SRU:**
  - SSR:
    - Single Board Computer (SBC)
    - Input/Output Card
    - Flash memory Card
  - SSMM Card
  - Power Supply (PS)
  - Hold-Up Card
  - Backplane
- **128 Mbits Flash Memory IC Used For Non-Volatile Memory**
  - SSR: 3.4 Gbits Of Good User Memory
  - SSMM: 132 Mbits Of Usable Storage Memory

MMU Architecture Diagram



External Electrical Interfaces

- **Power Source:**
  - 28 VDC Power Source At 7.5 Amp Maximum Current Capability Provided Through External Remote Power Controller (RPC)
- **SSR:**
  - Inputs:
    - Parallel Digital Format: E1, E2 And E3
    - Serial Digital Format: A1, A2 And B
    - Commands: MDM 16 Bit Discretes
  - Outputs:
    - T-O, FM Signal Processor (SP), KU Low Data Rate (LDR) And KU SP High Data Rate (HDR)
    - Status: MDM 28 Bit Discretes
- **SSMM**
  - uSMIA interfaces to GPC

Detailed MMU/Orbiter Interface Diagram